In the Claims:

Please amend the claims as indicated below:

1. (Original) A semiconductor device test pattern, comprising:

a word line on a semiconductor substrate;

an active region comprising a first impurity doped region and a second impurity doped region;

a first self-aligned contact pad electrically connected to the first impurity doped region;

a first bit line electrically connected to the first self-aligned contact pad;

a first probing pad electrically connected to the first bit line;

a second self-aligned contact pad electrically connected to the second impurity doped region;

a second conductive line electrically connected to the second self-aligned contact pad; and

a second probing pad electrically connected to the second conductive line.

2. (Original) The semiconductor device test pattern of Claim 1, further comprising:

a first direct contact electrically connected to the first self-aligned contact pad; and

a second contact electrically connected to the second self-aligned contact pad;

3. (Original) The semiconductor device test pattern of Claim 1, wherein the first self-aligned contact pad is one of a plurality of discrete first self-aligned contact pads disposed between the word line and a second word line.

4. (Original) The semiconductor device test pattern of Claim 1, further comprising an insulating pattern disposed between each of the first self-aligned contact pads disposed between the word line and a second word line.

5. (Original) The semiconductor device test pattern of Claim 1, further comprising a first metal contact between the first bit line and the first probing pad that electrically connects the first bit line and the first probing pad.

6. (Original) The semiconductor device test pattern of Claim 1, further comprising a second metal contact between the second conductive line and the second probing pad that electrically connects the second conductive line and the second probing pad.

7. (Original) The semiconductor device test pattern of Claim 1, wherein the second impurity doped region is one of a plurality of second doped impurity regions disposed between the word line and a second word line, and wherein the second self-aligned contact pad extends in a continuous line between the word line and the second word line to electrically connect to the plurality of second impurity doped regions.

8. (Original) The semiconductor device test pattern of Claim 1, wherein the first bit line is perpendicular to a major axis of the active region.

9. (Currently Amended) The semiconductor device test pattern of Claim 1, wherein the second conductive line ~~is a second bit line that~~ is perpendicular to the word line.

10. (Original) The semiconductor device test pattern of Claim 2, wherein the second contact is a buried contact.

11. (Original) The semiconductor device test pattern of Claim 1, wherein a major axis of the active region is at an oblique angle with respect to the word line.

12. (Currently Amended) The semiconductor device test pattern of Claim 1, wherein the second conductive line ~~is a second bit line that~~ is parallel to the word line.

13. (Original) The semiconductor device test pattern of Claim 1, wherein the first bit line and the second conductive line have a plurality of arms, and wherein one of the arms of the first bit line is disposed between each adjacent set of arms of the second conductive line.

14. (Original) The semiconductor device test pattern of Claim 1, wherein the second self-aligned contact pad is one of a plurality of discrete second self-aligned contact pads disposed between the word line and a second word line.

15. (Currently Amended) The semiconductor device test pattern of Claim 14 ~~13~~, wherein the second impurity doped region is one of a plurality of discrete second impurity doped regions disposed between the word line and the second word line, and wherein each of the second self aligned contact pads electrically connects to two of the discrete second impurity doped regions.

16. (Original) The semiconductor device test pattern of Claim 3, wherein the second self-aligned contact pad is one of a plurality of discrete second self-aligned contact pads disposed between the word line and a second word line, and wherein the one of the plurality of second self-aligned contact pads is disposed between adjacent of the first self-aligned contact pads.

17-40. (Withdrawn)

41. (Original) A semiconductor test structure comprising:

a semiconductor substrate including a plurality of active regions separated by isolation regions;

a plurality of parallel word lines on the semiconductor substrate with each word line crossing a plurality of the active regions;

an array of transistors on the semiconductor substrate, wherein each transistor of the array includes first and second source/drain regions on opposite sides of a respective of the plurality of word lines, wherein each word line separates the first and second source/drain regions of a plurality of the transistors of the array, and wherein each active region includes two transistors of the array sharing a common source/drain region;

a first bit line electrically connected to a first source/drain region of each transistor of the array; and

a second conductive line electrically connected to a second source/drain region of each transistor of the array.

42. (Original) A semiconductor test structure according to Claim 41 wherein the semiconductor substrate further includes a plurality of dynamic random access memory devices thereon.